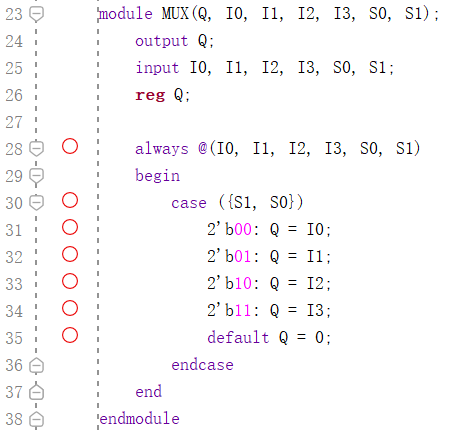
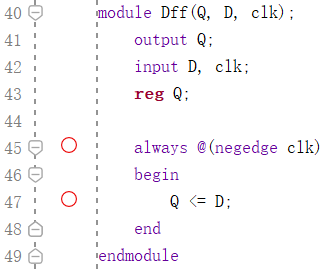
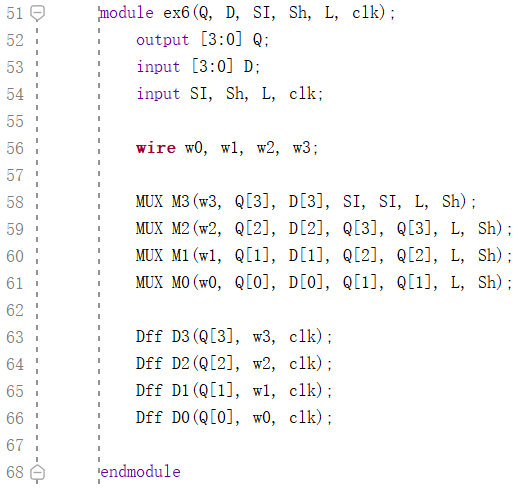
Q6.

Verilog Code:







Simulation Result:

